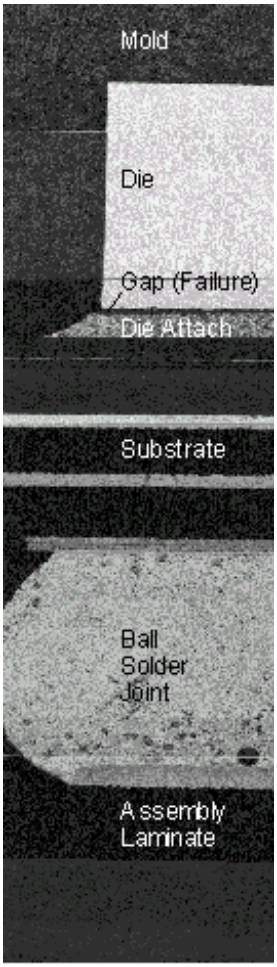
Reliability Analysis of Microelectronic Components and Materials

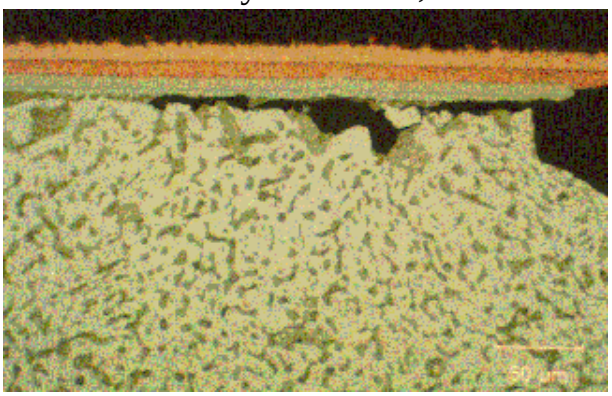


Increasing numbers of engineered products, across a wide range of sectors including aerospace and automotive, are dependent on the structural integrity of embedded micro-electronic components and assemblies.

Improved knowledge and modeling of the degradation processes relevant to soldered joints is crucial for more reliable life-cycle predictions. Joining methods are critical for the reliable use of electronic packages. In particular, since the advent of Surface Mount Technology (SMT) the reliability and lifetime of solder joints has been one of the paramount topics in the field of modern microelectronic packaging technology.

The first figure shows a cross-sectional cut through a Ball Grid Array (BGA), which provides some insight into the complexity and heterogeneity of SMT structures. Various materials are involved, each of which has to be joined reliably to its neighbor.

The second figure focuses on a eutectic SnPb solder joint of the BGA after 2000 thermal cycles between -20°C and +100°C. An interface crack has formed and propagates along the boundary to the pads made of copper, nickel, and gold. There are several reasons for the formation and the fatigue propagation of this type of crack. First, thermally activated elemental migration of the pad materials into the solder will take place, which leads to the growth of a relatively brittle intermetallic layer. Second, the various materials involved in a PBGA are not thermally matched and, therefore, residual stresses will be induced within the structure during thermal cycling. Third, the use of solder masks as well as the presence of interfaces in general will lead to a local intensification of these thermo-mechanical stresses, the so-called corner effect.



Due to the geometrical complexity and the non-linear material behavior involved finite element (FE) calculations are the only possibility to perform a transient heat conduction or stress-strain analysis of microelectronic

components. This was recognized very early and FE is now a well-established tool used by leading researchers in this field throughout the world.
The following rationale has proven to be an efficient way toward FE-results:

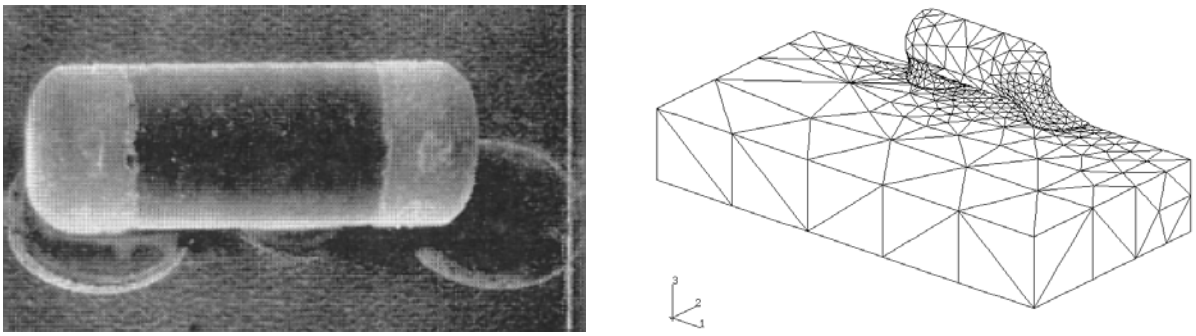
- The discretization of the structure is performed by means of a CAD-system, which allows creating an FE-mesh that can then be exported into the appropriate format of the FE-package. An example of such a CAD-tool is I-DEAS.

- The actual FE-calculation makes use of a commercial package, which, in our case, is the FE-code ABAQUS.

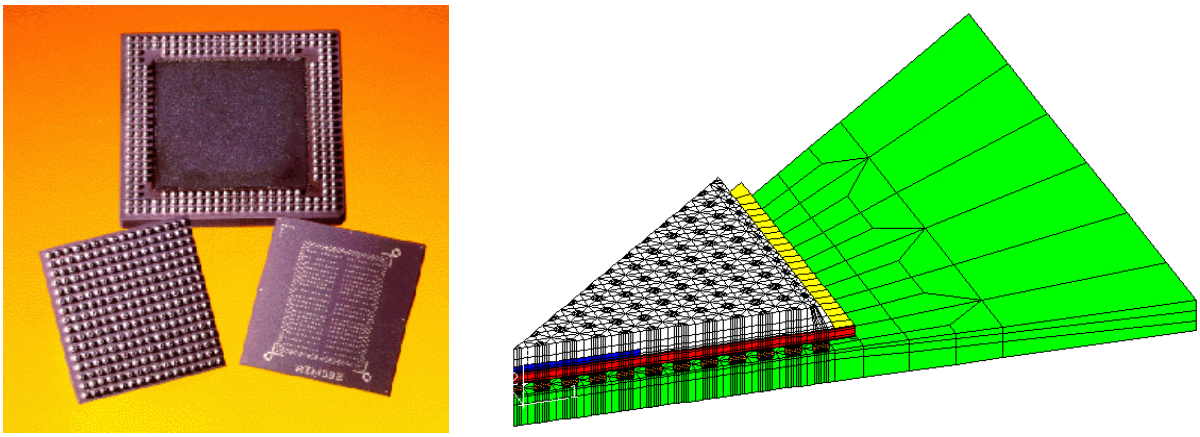
- Non-standard analysis features, for example the assessment of 3D-cracks by calculation of crack driving forces from the stresses and strains, need to be dealt with separately. Here it is advisable to create suitable post-processing tools, which make direct use of the data that can be obtained from the FE-package in question.

- Quite frequently microelectronic structures are extremely intricate and complex which makes a proper modeling of the whole structure impossible even if the most powerful computers are used. A possibility to obtain accurate information on the temperature as well as on the stress / strain state in local areas of interest is given by the so-called sub-modeling technique. Here, in a first step, a relatively coarse mesh is used to obtain global data which are the used as input during a second analysis performed on a detailed FE submodel.

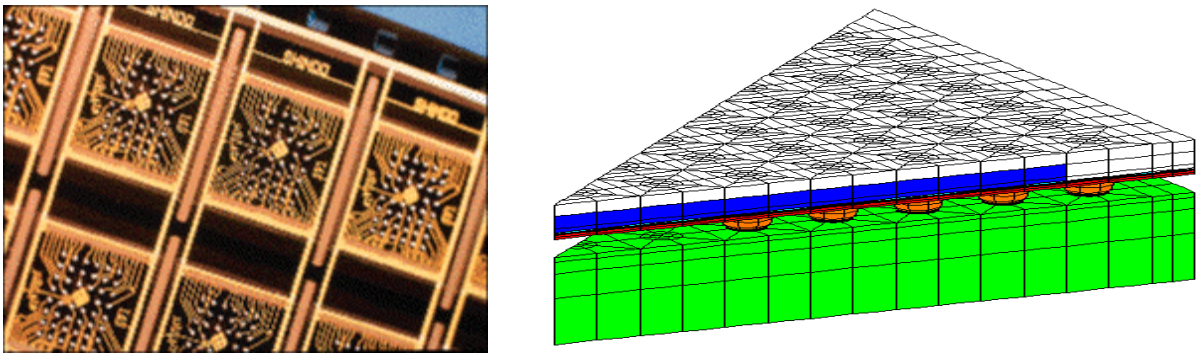
The following figures present a few examples of discretized micro-electronics structures, a MiniMELF resistor, a BGA variant, and a CSP.



Examples of CAD-use in microelectronics modeling: FE-meshes for a MiniMELF



Examples of CAD-use in microelectronics modeling: FE-meshes for a BGA



Examples of CAD-use in microelectronics modeling: FE-meshes for a CSP

A typical objective of an FE-analysis in micro-electronics problems is to predict the temperature field as well as the stress / strain distribution within the component, as they result from thermal loading (e.g., thermal cycling of the component according to military standards or power cycling, i.e., heat loss by the chip) and from mismatch of the various materials involved. Depending on the material behavior linear-elastic, visco-elastic, plastic, and visco-plastic constitutive laws are assumed during the calculation. As an example consider the solder used for the joining of a microelectronic component. If tin-lead solder is subjected to changes in temperature as well as to thermo-mechanical stresses it will react, on a meso-scale, with the formation and accumulation of irreversible visco-plastic strains and energies. As we shall see in the next section these strains or energies are used as a measure of the development of damage in the solder material. For the description of the material behavior of tin-lead solder (say) it is typically assumed that the increment of the total strain, $d\varepsilon_{ij}$, can additively be decomposed into four parts:

- elastic, $d\varepsilon_{ij}^{el}$, (reversible),
- plastic, $d\varepsilon_{ij}^{pl}$, (irreversible but independent of the loading rate),

- creep, $d\varepsilon_{ij}^{cr}$, (irreversible and dependent on the loading rate), and
- thermal, $d\varepsilon_{ij}^{th}$,

as follows:

$$d\varepsilon_{ij} = d\varepsilon_{ij}^{el} + d\varepsilon_{ij}^{pl} + d\varepsilon_{ij}^{cr} + d\varepsilon_{ij}^{th}$$

.

In order to compute the contribution of irreversible plastic deformation to the strain the Prandtl-Reuss equations of time-independent J_2-plasticity are solved:

$$d\varepsilon'_{ij} = \frac{1}{2G} dS_{ij} + \frac{3d\varepsilon_e^{pl}}{2\sigma_y} S_{ij}$$

,

where the dash refers to the deviatoric part of the infinitesimal strain tensor, ε_{ij}, G is the shear modulus, S_{ij} denotes the deviatoric part of the stress tensor, i.e.:

$$S_{ij} = \sigma_{ij} + p\delta_{ij}$$

,

$$p = -\frac{1}{3}\sigma_{ij}$$

.

ε_e^{pl} is the current equivalent plastic strain:

$$\varepsilon_e^{pl} = \int \sqrt{\frac{2}{3} d\varepsilon_{ij}^{pl}\, d\varepsilon_{ij}^{pl}}$$

,

and σ_y denotes the current yield stress which is determined as a function of equivalent plastic strain from uniaxial loading experiments. Frequently a von Mises yield criterion is used for evaluation together with a linear isotropic strain hardening. To this end the corresponding material data need to be available, knowledge of which is often inaccurate and insufficient. This is not only because microelectronics materials involved are sometimes relatively "new" and, therefore, unexplored but also because of the following reasons. Often bulk specimens are used for testing and the resulting material parameters are only of limited use for the description of a miniaturized component. Moreover, the materials usually age and their material parameters will change over time. Again, solder is a prominent example as we shall see in the upcoming sections.

For the mathematical description of the change in strain due to thermal loading isotropic material behavior is assumed:

$$d\varepsilon_{ij}^{th} = \alpha dT \delta_{ij}$$

.

In this equation α represents the coefficient of linear thermal expansion, dT is the change in temperature, and δ_{ij} denotes the Kronecker tensor.

For isotropic materials the creep strain rate is often described by a hyperbolic flow rule:

$$\dot{\varepsilon}_e^{cr} = A[sinh(B\sigma_e)]^n e^{\left(-\frac{\Delta H}{R\theta}\right)}$$

,

where A, B, n are material constants, ΔH is the activation enthalpy, R is the gas constant, and θ denotes the absolute temperature. Moreover, the equivalent stress, σ_e, is defined as follows:

$$\sigma_e = \sqrt{\frac{3}{2} S_{ij} S_{ij}}$$

.

Once the stresses and irreversible strain rates are known they can be used to obtain the corresponding dissipated energy densities:

$$W^{pl} = \int \sigma_{ij}\, d\varepsilon_{ij}^{pl}$$

,

$$W^{cr} = \int \sigma_{ij}\, d\varepsilon_{ij}^{cr}$$

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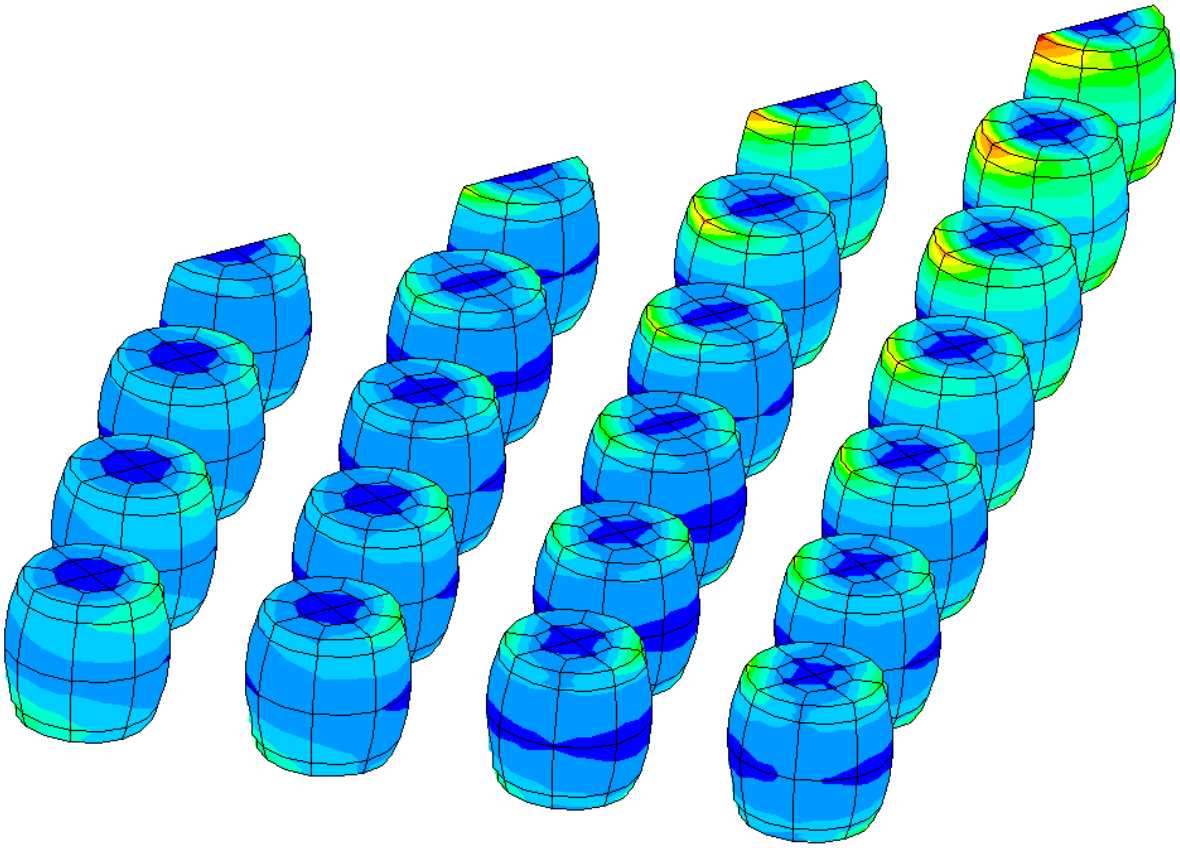

Accumulation of creep strain in the solder bumps of a CSP as a consequence of thermal cycling.

In this field of research we collaborate with Siemens AG and Infineon in Berlin and Munich and Professor O. Hahn's group at the Laboratorium für Werkstoff- und Fügetechnik at the University of Paderborn in Paderborn/Germany.